

AIO_x - ALD applications for silicon solar cells edge passivation

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The use of smaller size crystalline silicon (c-Si) solar cells to improve module power output has been well established. This alternative interconnection method, from half-cells to *shingle* architectures, indeed allows reduced resistive losses, cells shadowing and spacing, leading to a module power increase up to 10%_{rel.} [1]. However, the reduction of the cell perimeter over area ratio makes it more sensitive to edge effects, especially for high efficiency solar cells [2]. Furthermore, the most industrial-adapted way to obtain such smaller cells is to cut conventional ones, creating unpassivated edges: highly recombining areas for charge carriers. The combination of these two significant drawbacks can lead to an edge induced cell efficiency loss close to 1%_{abs.} [3], bringing out the interest of a passivation step. To address this challenge, thermal Atomic Layer Deposition (ALD) of aluminium oxide (AIO_x) appears to be one of the most promising technique, due to its high surface passivation level and its ability to be adapted as an industrial post-metallisation process [4].

Before assessing the effect of such procedure on complete cell architecture edges, it has been decided for this work to firstly focus the assessment on full-area c-Si(n) precursors. After polishing and cleaning the wafers in KOH solution, variable thicknesses of AIO_x (TMA/H₂O) layers have been deposited using an innovating PPW-ALD tool from ENCAPSULIX. The particularity here is the *Parallel Precursor Wave architecture*, i.e a laminar gas flow, allowing an improved yield suited to the industry [5]. As-dep ALD AIO_x showing little to no passivation on this kind of precursors, we studied different conditions of post-deposition annealing in a conventional furnace under N₂ gas flow. The passivation quality is evaluated by photoluminescence, as its signal is correlated to carrier's recombination. As expected from the literature, passivation level increases with the temperature and also with the AIO_x thickness (Fig.1). Secondly, we checked the edge passivation of c-Si samples already passivated with poly-Si/SiO_x after cutting, conventional thermal ALD (BENEQ) and annealing. The photoluminescence signal of the edge (Fig.2) indicates that the AIO_x edge passivation is effective.

In further investigation, we will assess the precursor and metallised solar cell edge passivation by AIO_x elaborated by PPW-ALD compared to improved conventional thermal ALD and alternative annealing conditions.

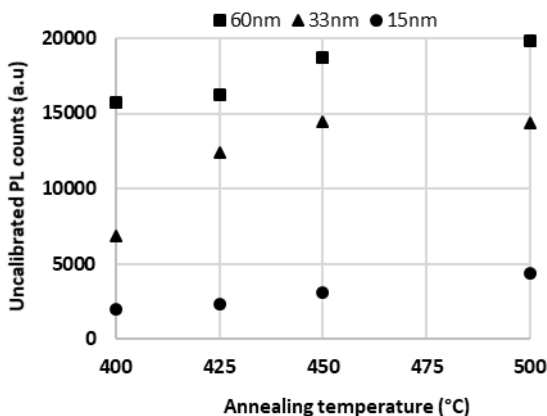


Figure 2 : Full area mean PL signal. ENCAPSULIX AIO_x deposition on Si(n) Cz, 2-3Ωcm, with KOH etched surface precursors. Annealings of 10 min in a conventional furnace.

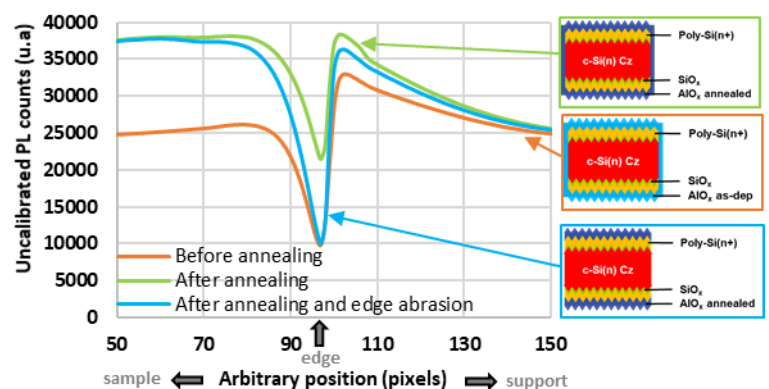


Figure 1 : Profil PL signal (1cm=70pixels). Conventional thermal ALD AIO_x (BENEQ) on polySi/oxyde textured precursors. This figure shows the profil signal before, after annealing at 350°C for 10min and after abrasion of the edge with sandpaper.

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[3] V. Giglia, et al, Influence of Edge Recombinations on the Performance of Half-, Shingled- and Full Silicon Heterojunction Solar Cells. 37th European Photovoltaic Solar Energy Conference and Exhibition, 2020

[4] P. Baliozian et al, Postmetallization "Passivated Edge Technology" for Separated Silicon Solar Cells, IEEE JPV, Vol. 10, N. 2, March 2020

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